Hardware Developments for the Low Level RF System in the TESLA Test Facilities

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1. INTRODUCTION

The RF Control System for the TESLA Test Facility (Figure 1), its principles, features and operational aspects were presented in many publications [1], [2], [3] and [4]. This paper gives a short description of some electronic modules developed in-house and used in the digital feedback, diagnostics and exceptional handling of the System.

2. FAST DIGITAL FEEDBACK HARDWARE

The hardware part of the digital feedback consists of 14-bit ADCs operated at a sampling rate of 1 MHz, five DSPs (TMS320C40, floating-point processing) and two 16-bit DACs which drive the vector modulator. DSPs are mounted on TIM-40 modules. The commercial carrier board is DBV44 from Blue Wave Systems. It can accommodate up to four such modules. The data transfer of 32-bit words between ADC, DSP and DAC boards is performed through the communication port links on a byte-to-byte basis at a maximum rate of 20 MB per second.

2.1 Four-Channel ADC Board (ADC-4)

Features:

- four independent 14-bit sampling A-D converting channels with data transfer to DSP communication ports (TMS320C40);
- for each A-D channel:
  - +/- 170 mV full-scale input signal
  - preamplifier: gain **- 28**
    bandwidth **- 9.0 MHz**
    pp-Noise **- 3 mV**
  - 14-bit resolution
  - 320 ns time of conversion
  - 2 MHz maximum sampling rate
- 450 ns data transfer time from pair of channels to the DSP commport.

Description

ADC-4 schematics (Picture 2) is mounted on the Euromechanical card 6U, single width. It consists of four identical A-D channels.

The analog part includes a 3-stage preamplifier (AD797 and AD843) with a common gain of 28, connected to a 14-bit ADC chip AD929. The forth stage is a follower for monitoring ADC chip input signal in an external connector. The ADC board takes single ended signals from RF down converters. The connection between preamplifiers and ADC chips is AC coupled (250 kHz signal is measured).

The digital part of the schematics is based on a PLD chip MACH435. It is an interface between two ADC chips, external timing (Start, 1 MHz clock and Reset signals) and a DSP communication port. The interface performs the following functions:

- provides timing signals for the ADC chips during a defined time period (2048 * 1 mks)
- takes data from ADCs in integer format and converts it into floating-point format before sending it to the DSP board
- supports the handshake protocol of the data transfer procedure in a DSP commport link.

The two LEDs on the front panel indicate the condition of the data transfer through the commport link (DTR), and the presence of the Start and 1 MHz pulses from the system timing (ST).

2.2 Two Channel DAC Board (DAC-2)

Features:

- a two channel digital-to-analog converter controlled through the DSP (TMS320C40) commport,
- for each channel:
  - +/-5 V full-scale output signal (R = 50 Ohm)
  - 16-bit resolution
  - max 2 MSPS update rate
  - 120 ns output signal rise/fall time (10% to 90%)
  - 2 mV p/p Noise

Description

The DAC-2 schematics (Picture 3) is placed on the Euromechanical card 6U, single width. It includes two identical D-A channels and a common interface between them and the DSP commport. Each analog channel is based on a 16-bit DAC AD768. Current values on its outputs (A - direct output, B - complement one) correspond to incoming data in accordance with the following equation:

$$I_{out} = (DAC\ CODE / 65536) * 4\ I_{ref}$$

To have a bipolar mode of operation, both of them drive an operational amplifier with a current booster (HA2525 and HA5002). This amplifier has to work on a long-length coax cable. That is why a 125 mA fuse is used to prevent its damage from occasional shortcuts. Two trimmers implemented in the schematics are necessary to tune the output zero level (Offset) and amplitude (Ampl) of the analog signal.

The interface between the two DACs and the DSP board is based on a PLD chip MACH435, which performs the following functions:

- supports the DSP commport handshake protocol during the data transfer procedure,
- converts incoming data from the floating-point format (used for calculations in DSP) to the integer one, which can be interpreted by DAC chips,
- checks incoming data on permitted for DACs diapason.

In the case when incoming data values exceed this diapason, MACH435 writes into defined DACs codes corresponding to either maximum (+5V) or minimum (-5V) output signal levels. Such situations are reflected in conditions of monitoring output signals "Data Exc1" and "Data Exc2" and the LEDs (red) which correspond to them. Positive exceeding of data gives +3V level, negative data exceeding - 0V, normal data corresponds to +1.5V. The LEDs are driven by data exceedings of both types. The condition of data transfer through the commpot link is reflected by LED "DTR" (green).

The timing diagram of the data transfer in commport links between ADC, DSP and DAC boards is shown in Picture 4.

Presented signals are:

- StConv - Start of Conversion in the ADCs
- EOC - End Of Conversion in the ADC chips (fall edge)
- STRB adc - data transfer strobe pulses from ADC-4 to DSP board
- STRB dsp - data transfer strobe pulses from DSP board to DAC-2

3. TWO-CHANNEL FUNCTIONAL GENERATOR FG-2

This board performs the functions of the IQ-driver in the Local Oscillator (Picture 1). Supplied by F ref = 9 MHz, it produces two 250 kHz signals, which are phase-shifted at 90°; their values are defined by the tables loaded in RAM blocks. These signals are real and imaginary components to drive a vector modulator with input frequency F rf = 1300MHz.

As a result, the Local Oscillator produces the RF diagnostic frequency, which is 250 kHz above the RF operating frequency and equals

$$F_{lo} = (144 + 1/36) * F_{ref}$$

The LO frequency is then used in down-converters to select 250 kHz intermediate signals from the field probes of the RF cavities.

3.1. Board Description

The Two-Channel Functional Generator Board (FG-2) is a two-channel (N0 and N1) generator of analog signals, every one of which can be written in digital form into the corresponding memory block (MEM0 and MEM1). The changes of the addresses of memory cells in both blocks are made synchronously, from a single source called the Address Counter (AC). The initial data is written into the AC either directly from the bus or through a special register (Low Register - LR). The Address Counter has an increment mode. Its state changes either at getting a count pulse from the divider (DVD) of the control frequency or at the reference to the memory blocks with WR/RD incrementing commands. The cycle of the address counter is defined by the data written into the LR and High Register - HR.

The data stream from the memory blocks into DACs can be checked by fixing the data (at "random" time) into the intermediate registers Address Register (AR), DATA_0_Register (data for DAC0) and DATA_1_Register (data for DAC1) with the command WRDATA_ADDR. These three intermediate values are then available for reading. The frequency divider is used to form a countable series for the Address Counter from the control frequencies (Ext. Clock or Int. Clock). The dividing coefficient is loaded in the Divider Register DVDR. The synchronization of the scheme with external processes is made by the pulse Ext.Reset. The Int.Reset is used in case such synchronization is not necessary. Signals corresponding to cycles of DVD and AC are placed on the front panel.

The Cycle Counter CC generates external pulse (CCout) and forms the interrupt request to the bus delayed from RST pulse. This delay is defined by both values loaded to CCR and CC count clock. It is possible to fix the intermediate condition of CC in CCOR and to read it later. The interrupt logic is standard. The value of STATUS/ID register is defined by jumpers (8 bits).

3.2. Board Specification

1. Number of channels	2
2. Modes of Work:	
- Continuous	
- One Cycle	
- Direct Write to DACs from Bus	
3. Output Parameters for each channel:	
- Output Voltage Rate	+/- 5 V
- Max Rated Current	+/- 100 mA (R = 50)
- pp Noise	<= 2 mV
4. Transfer Parameters:	
- Amplitude Resolution	16 bits
- Min Time Resolution	66 ns
- Output Setting Time	120 ns (10% - 90%)
5. Memory Size for each Channel:	32K short (16 bit) words
6. External Signals:	
- Ext Clock	<= 16 MHz
- Ext Reset	depends on Clock and memory size used
7. VME Interface:	
- Board Type	slave
- Addressing Mode	A16
- Data Transfer	D16
- VME Interrupt	End of Cycle
8. Power Supply:	
+ 5 V	0.9 A
+ 12 V	0.3 A
- 12 V	0.3 A

3.3. Control and Status Registers

Control Register - CR (16 bits)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NU	NU	NU	IRQ Enbl	NU	Cycle_Cntr OUT		IN	Addr Cntr		NU	DAC_Strb 1	0	SELECTION Clck		Rst

CR bits:

Bit 0 (0 - Int. Reset, 1 - Ext. Reset)
Bits 1-2 (00 - Clocks Disable, 01 - Ext. Clock, 10 - Int. Clock)
Bit 3 (0 - DVD output, 1 - WRDAC0)
Bit 4 (0 - DVD output, 1 - WRDAC1)
Bit 6 (1 - MEMory Reading to DACs, 0 - MEMory Preparation)
Bit 7 (0 - Continuous Mode, 1 - One Cycle Mode)*
Bits 8-9 (00 - Input Closed, 01 - AC Input Used, 10 - AC Output Used)
Bit 10 (1 - CC Out Enable, 0 - CC Out Disable)
Bit 12 (1 - Interrupt Request Enable, 0 - Interrupt Request Disable)

Notes:
Write Command to CR (WRCR):
- releases Flag of Cycle Counter
- gives permission for DAC strobes (after Sys Reset)
- terminates clocks inside the board

Status Register - SR (16 bits)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sys Rst	NU	IRQ		Cycle Counter Out		In		Address Counter		NU	DACs 1	0	Clk Cond	Clk	Extern. Rst

SR bits:

Bit 0 (0 - Ext. Reset No, 1 - Ext. Reset Yes)
Bit 1 (1 - Ext. Clock Yes, 0 - Ext. Clock No)
Bit 2 (1 - CLK Enable, 0 - CLK Disable)
Bit 3 (1 - DAC0 is in Progress, 0 - DAC0 is not in Progress)
Bit 4 (1 - DAC1 is in Progress, 0 - DAC1 is not in Progress)
Bit 6 (1 - MEMory Reading DACs, 0 - MEMory Preparation)
Bit 7 (1 - One Cycle Mode, 0 - Continuous Mode)
Bits 8-9 (00 - CC Input Closed, 01 - AC Input Used, 10 - AC Output Used)
Bit 10 (1 - CC Out Enable, 0 - CC Out Disable)
Bit 11 (1 - CC is in Progress, 0 - CC is not in Progress)
Bit 12 (1 - Interrupt Request Enable, 0 - Interrupt Request Disable)
Bit 13 (1 - CC Flag ON, 0 - CC Flag OFF)
Bit 15 (1 - After Sys Rst, 0 - No Sys Rst)

4. DSP INPUT/OUTPUT REGISTER

The DSP I/O Register (Picture 6) is a board which makes it possible to extend the functions of the DSP module taking digital information from some system devices and sending the result of calculation to other devices by using only one commport. This function belongs to the regular part of the schematics. The special part of the board allows the DSP, which is responsible for generating exceptional handling commands, to notify the Beam Interlock System. There are two situations when the IO register sends a block signal to the fast Beam Interlock System:

- in case of the RF System failure (the DSP board which analyzes the current control parameters defines this moment and issues an exceptional interrupt)
- the DSP board does not reply to the request from the IO Register

Description

The input registers IR0 – IR2 are used to fix incoming data and transfer it into the DSP commport. Two external pulses are implemented for these operations:

- WR writes information from DATA IN connector into registers IR1 and IR2
- CS (Check Strobe) has pulse duration of 8 μs, its rise edge writes "1s" in IR0 and fall edge – "0s"
  In reality, this pulse gets the Edge Selector block where it is converted to a set of short pulses N1+N2, N1 and N2.

Under normal condition, the commport link is under the DSP control, which is ready to send data to the register board at any time. However, the Logic of Direction locks the commport link every time WR and N1+N2 pulses appear to send data in the byte-to-byte manner. The standard commport data message includes four bytes (in our case, the last byte is presented by 1s – hFF). Each data byte is followed by STRB pulse. The DSP replies to it with the RDY signal (readiness to receive the next byte). All signals in the DSP commport link are bidirectional.

The output register is used to keep the data received from the DSP board. The first byte is loaded to OR0, two following bytes are placed in OR1 and OR2, and the forth byte is ignored by the board. Outputs of OR1-OR2 registers are directly wired with DATA OUT connector.

The Exceptional Handling command takes up only part of the DSP message directed to the IO register board, and it is placed in OR0. A special logical block is attached to the outputs of OR0 in order to generate true signals for the Beam Interlock System. This block which takes into account the OR0 contents and the time position of the Check Strobe edges keeps on its four outputs EN0-EN3 levels which correspond to of both the RF System and the DSP board. Picture 7 displays two modes of generating enable/disable signals for the Beam Interlock System: A – during the RF system failure and B – during DSP failure.

The enable signal as a 20 mA current along a two-wire cable (current loop) indicates normal operation, and a lack of it means an RF System malfunction. The current driver is connected to the logical block via optocouplers, with its four outputs wired to 2-pin LEMO connectors. The current status of system of the board is reflected by four LED pairs on the front panel.

5. TRANSIENT DETECTOR BOARD

The calibration of the vector-sum and the phasing of the cavities is based on beam loading. The beam induced transients are observed at zero crossing and phase offsets are determined by nulling of the average transients. A device which allow to detect and amplify signals of the beam induced transients is called the Transient Detector board (Pic.e 8).

Its features:

- four independent channels in Euromehanics form factor
- common sample/hold timing
- for each channel:
  - 1.5MHz bandwidth
  - variable gain of 25; 50; 75 and 100
  - p/p Noise of 15 mV (max gain)

Discription

A RF field probe signal of cavities is used for this board. After the peack detector, which is based on the Schottky diode BAT62 (point A) it looks like as the gradient signal with a typical level of 5V at a gradient of 25 MV/m. This signal gets through a buffer U1 to a sample & hold IC U2. Just before the beam pulse arrives a timing control signal Sample/Hold memorizes a level of the gradient signal into U2, after that it is inverted by an amplifier (with small gain) U3. Subtraction of both real and memorized gradient signals takes place on summing resistors (B node). The resultant signal is amplified by ICs U5 and U6. The output signals can be monitored by a scope or degitized by analog-to-digital converters.

ACKNOWLEDGEMENTS

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DESIGN OF THE DIGITAL RF CONTROL SYSTEM FOR THE TESLA TEST FACILITY.

[2] A. Gamp, S. Goloborodko, M. Liepe, T. Plawski, K. Rehlich, T. Schilcher, S.N. Simrock and Y. Tchernoousko.
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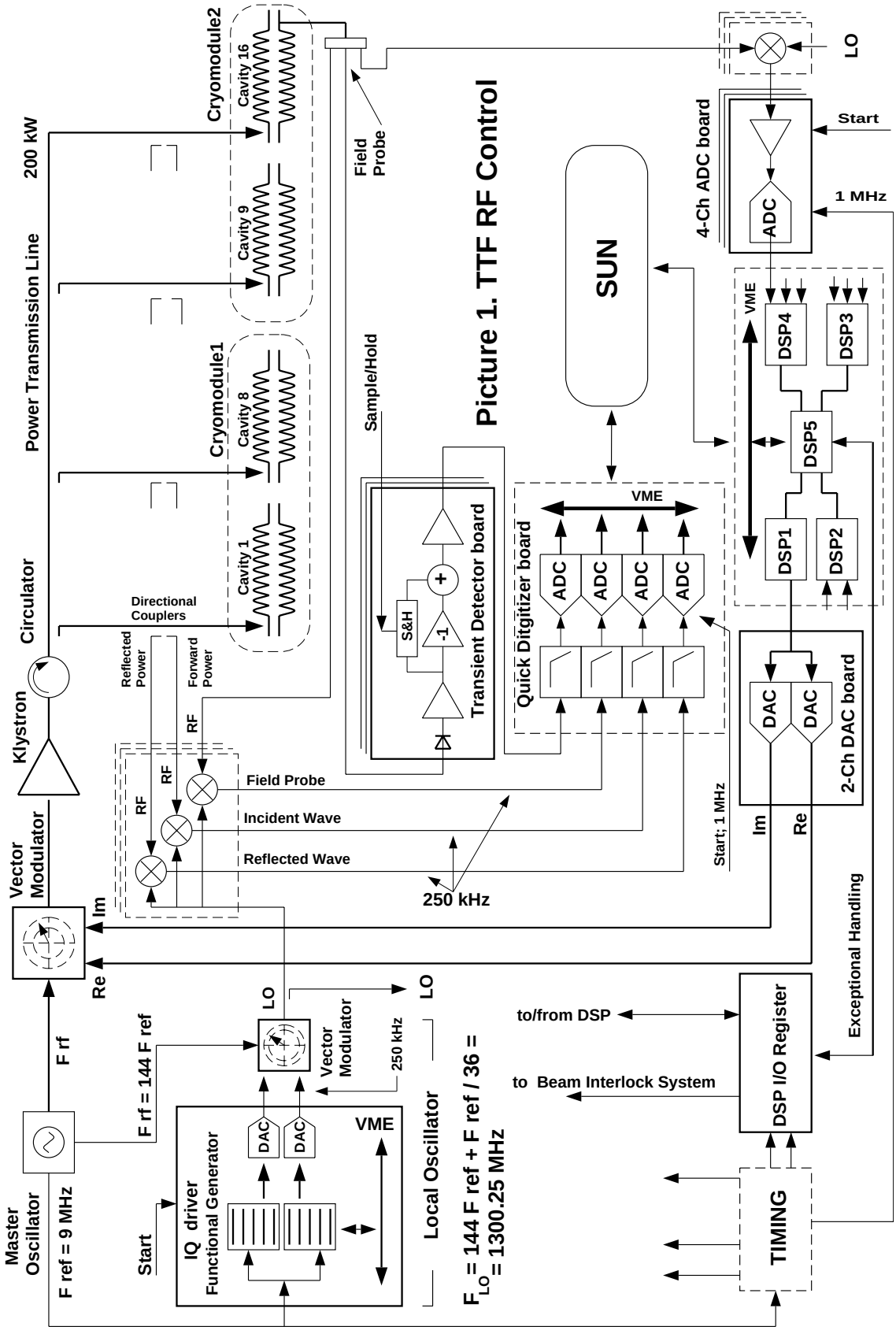
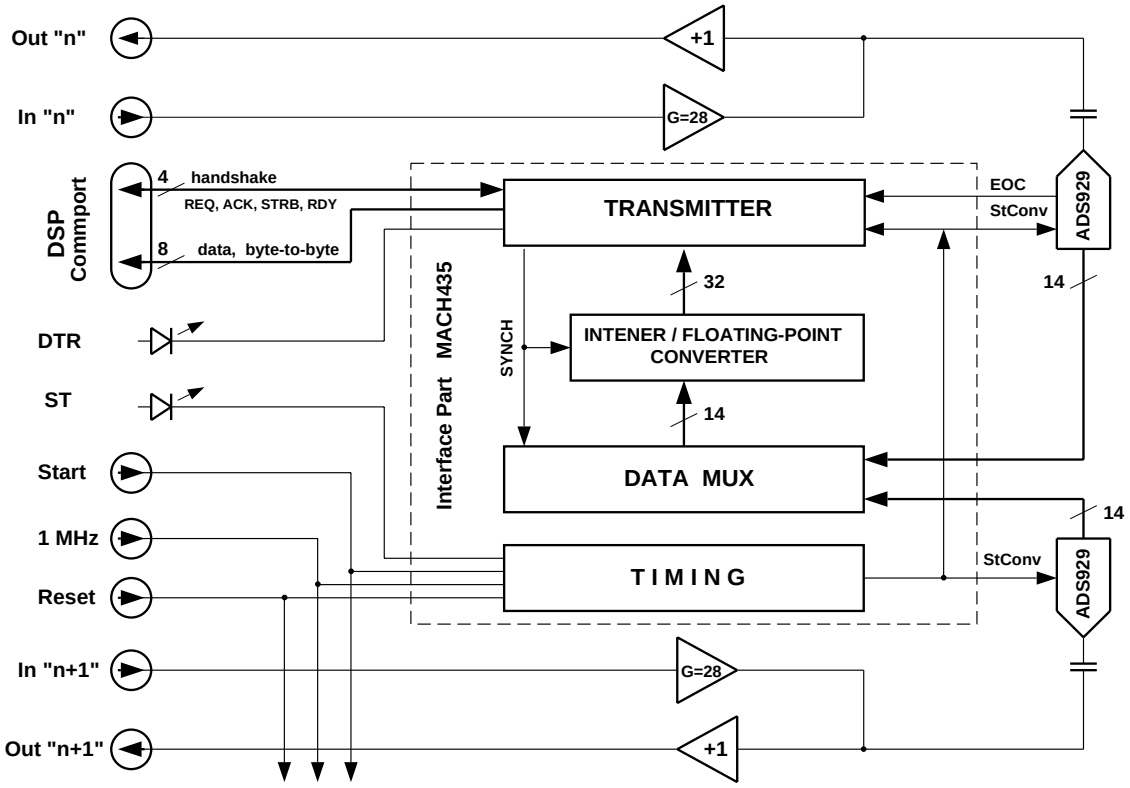
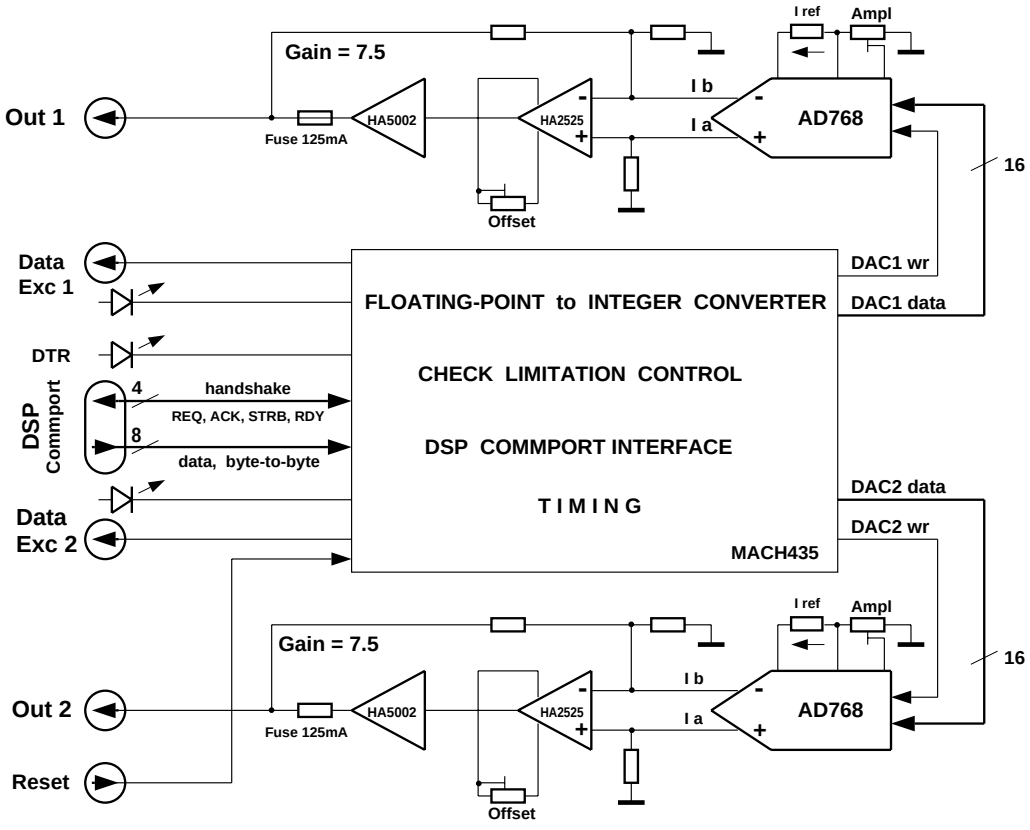
[4] T. Schilher.
VECTOR SUM CONTROL OF PULSED ACCELERATING FIELDS IN LORENTZ FORCE DETUNED SUPERCONDUCTING CAVITIES.

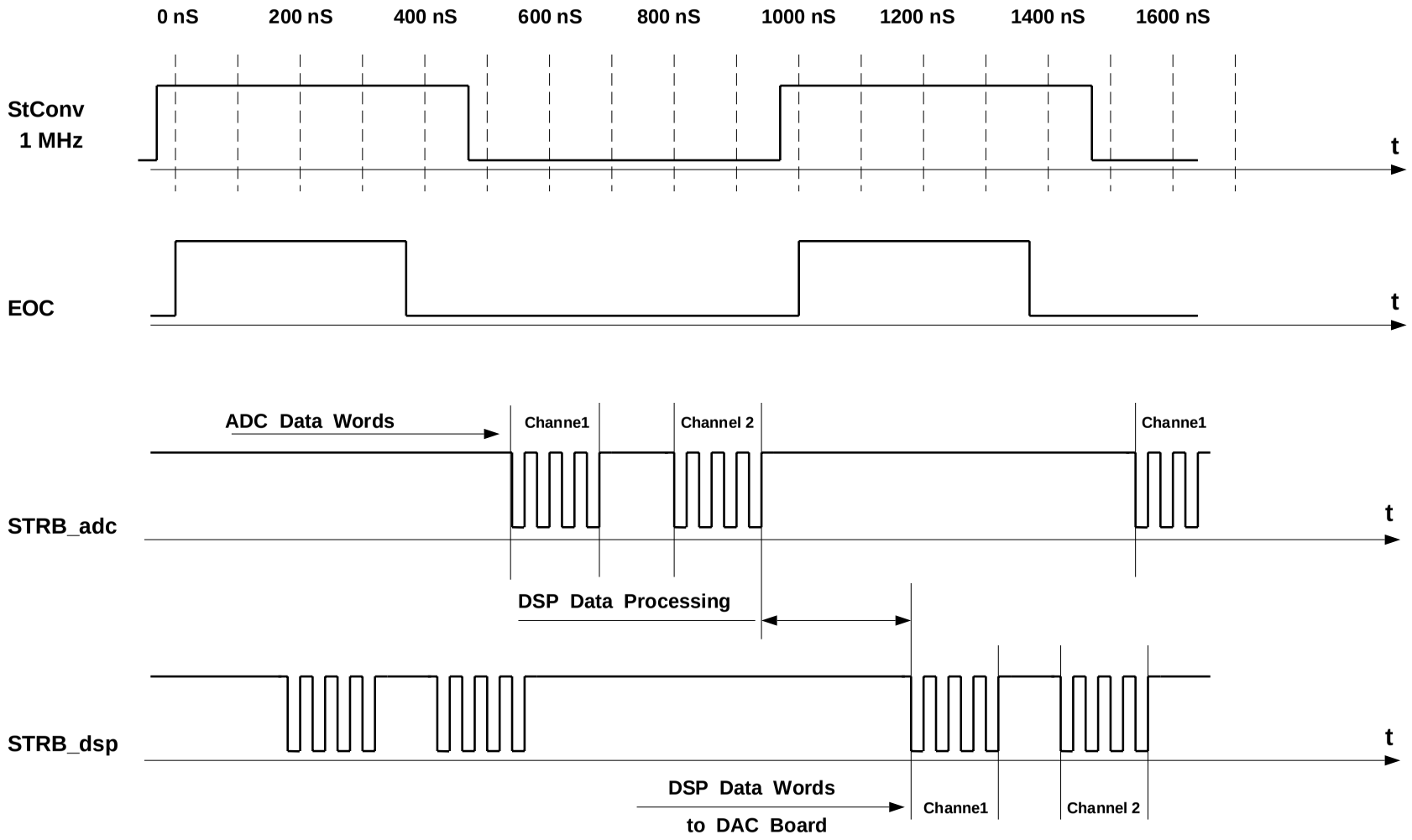

Picture 1. TTF RF Control
Cryomodule2
Cavity 16
Cavity 9
Cryomodule1
Cavity 8
Cavity 1
Power Transmission Line
200 kW
Circulator
Klystron
Directional Couplers
Reflected Power
Forward Power
RF
Field Probe
Incident Wave
Reflected Wave
250 kHz
Vector Modulator
Im
Re
Master Oscillator
F ref = 9 MHz
F rf
F rf = 144 F ref
LO
Vector Modulator
250 kHz
Local Oscillator
F_{LO} = 144 F ref + F ref / 36 = = 1300.25 MHz
IQ driver Functional Generator
DAC
VME
Start
Sample/Hold
S&H
-1
Transient Detector board
Field Probe
SUN
Quick Ditgitizer board
ADC
VME
4-Ch ADC board
Start
1 MHz
DSP4
DSP3
DSP5
DSP1
DSP2
2-Ch DAC board
Start; 1 MHz
Exceptional Handling
to/from DSP
to Beam Interlock System
DSP I/O Register
TIMING



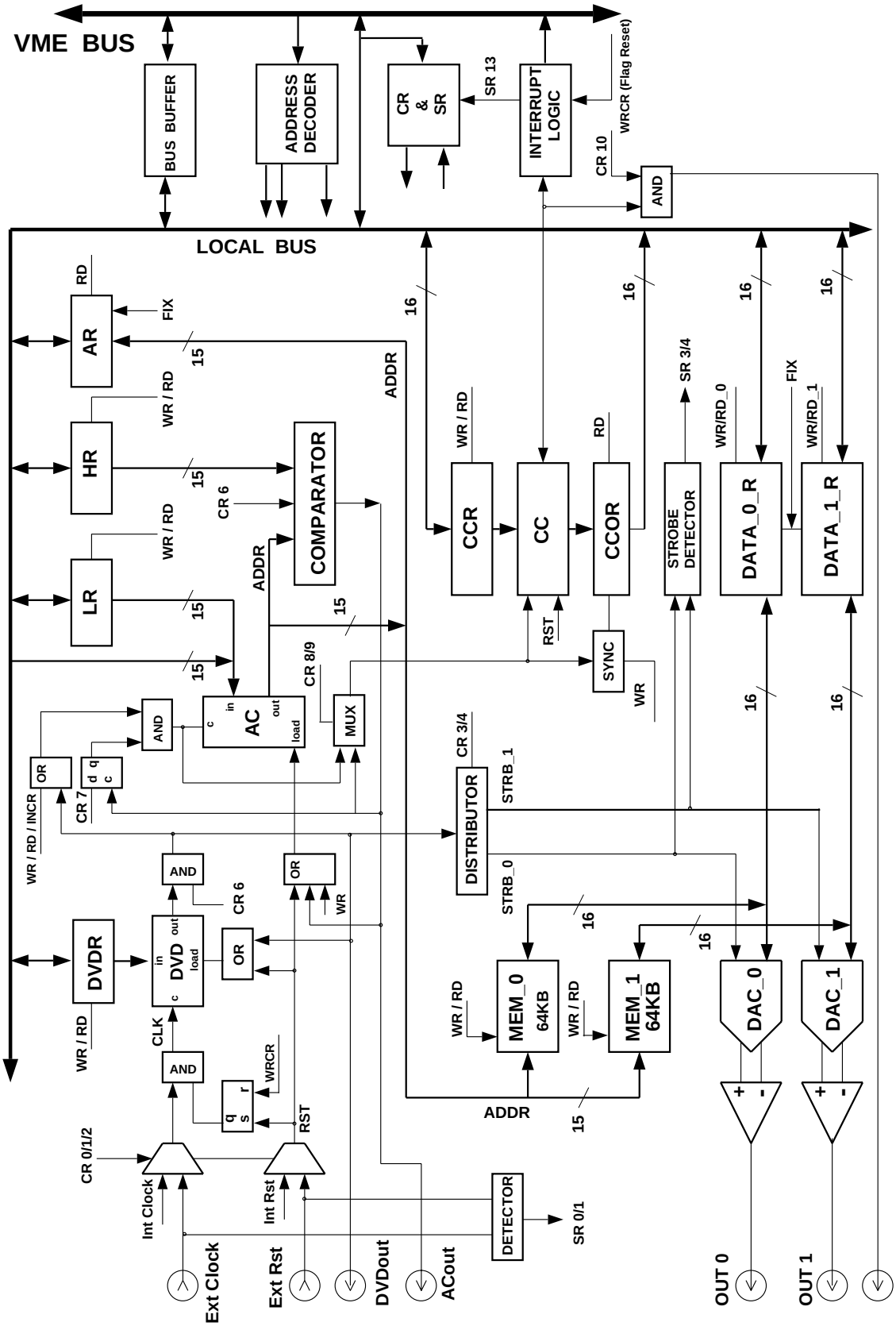
Picture 2. ADC-4 board (a half of schematics)



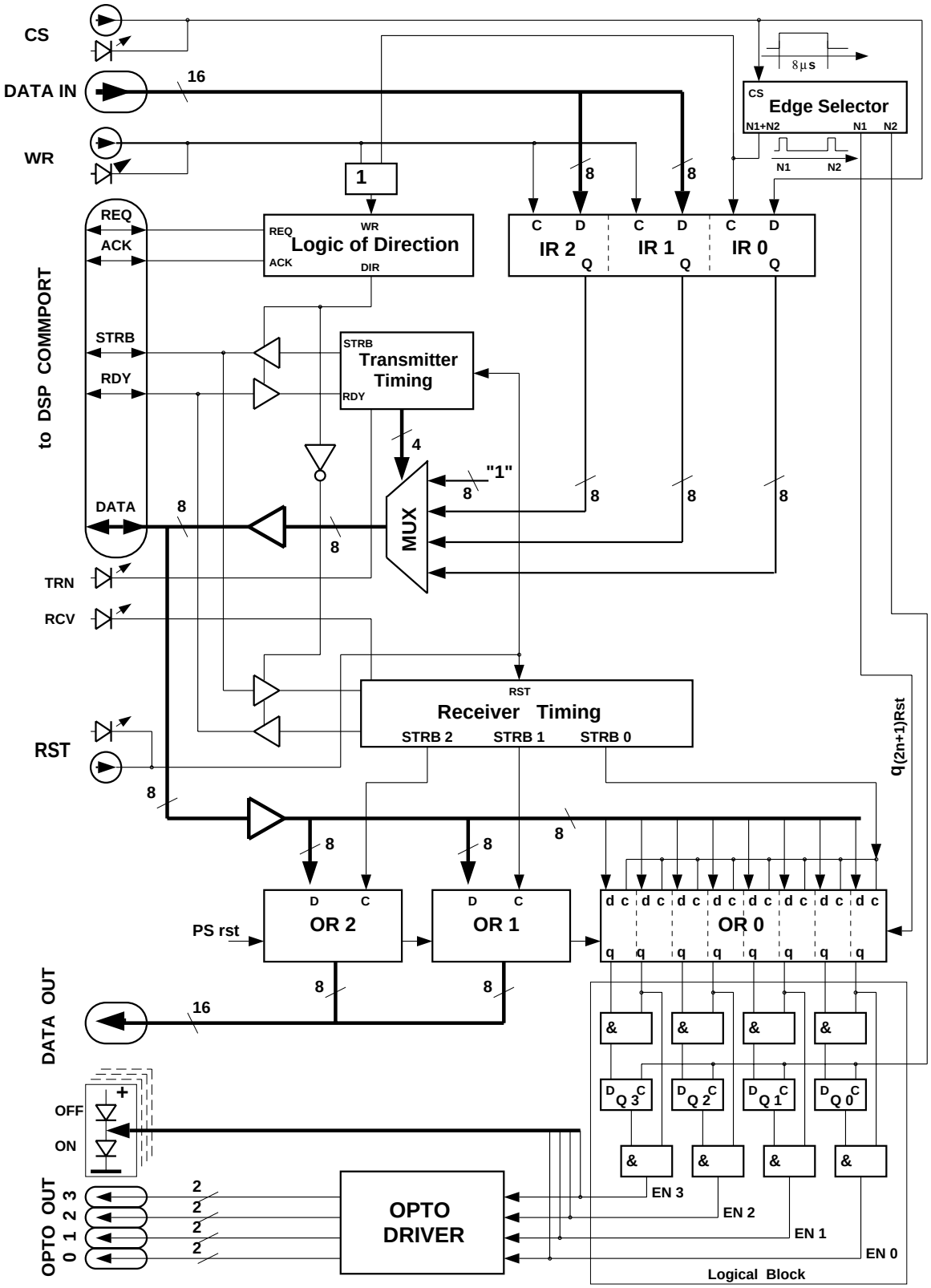
Picture 3. DAC-2 board



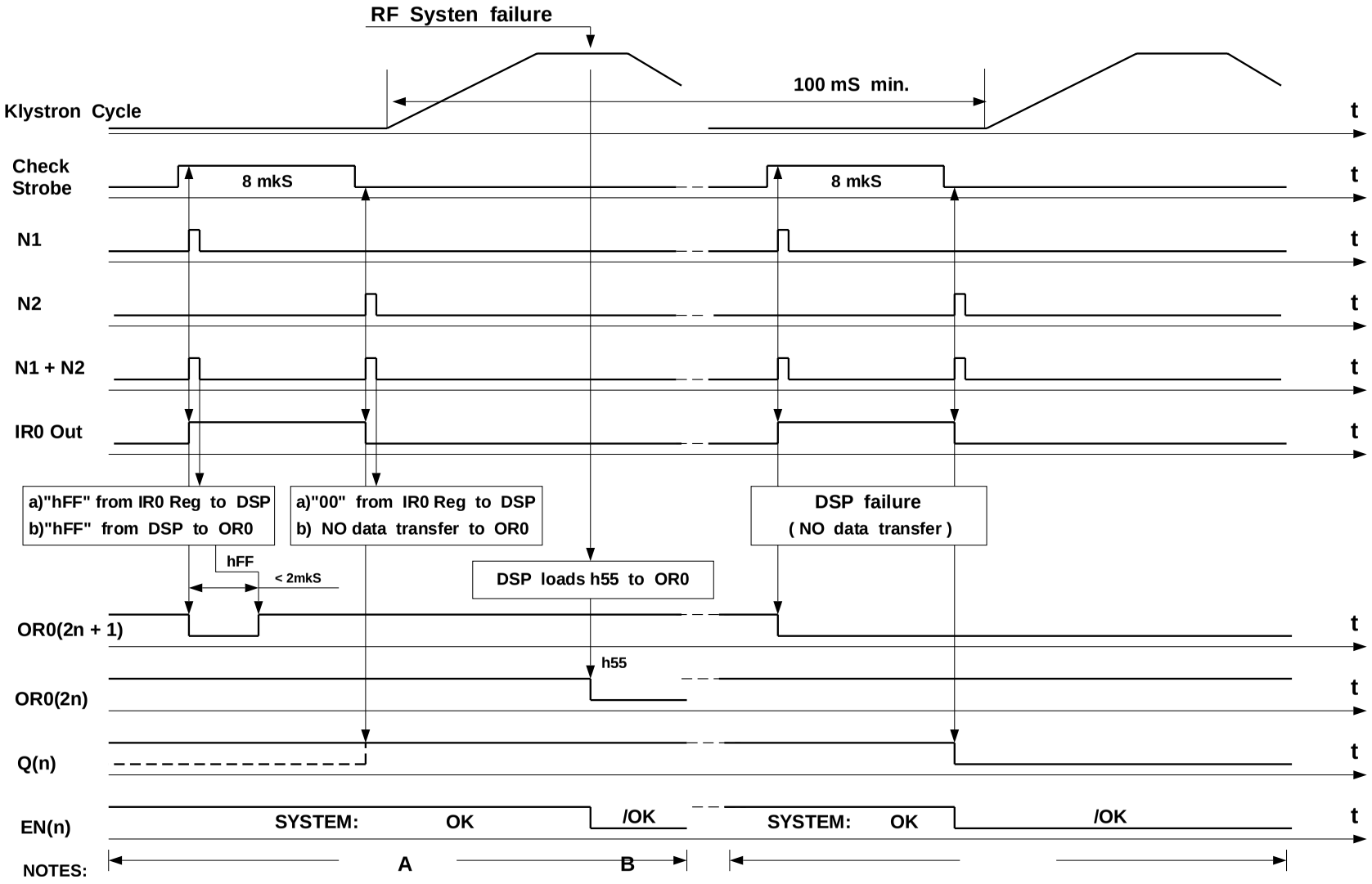
Picture 4. Timing Diagram of Data Strobes in ADC - DSP and DSP - DAC Commport Links.



Picture 5. 2 - channel Functional Generator FG-2.

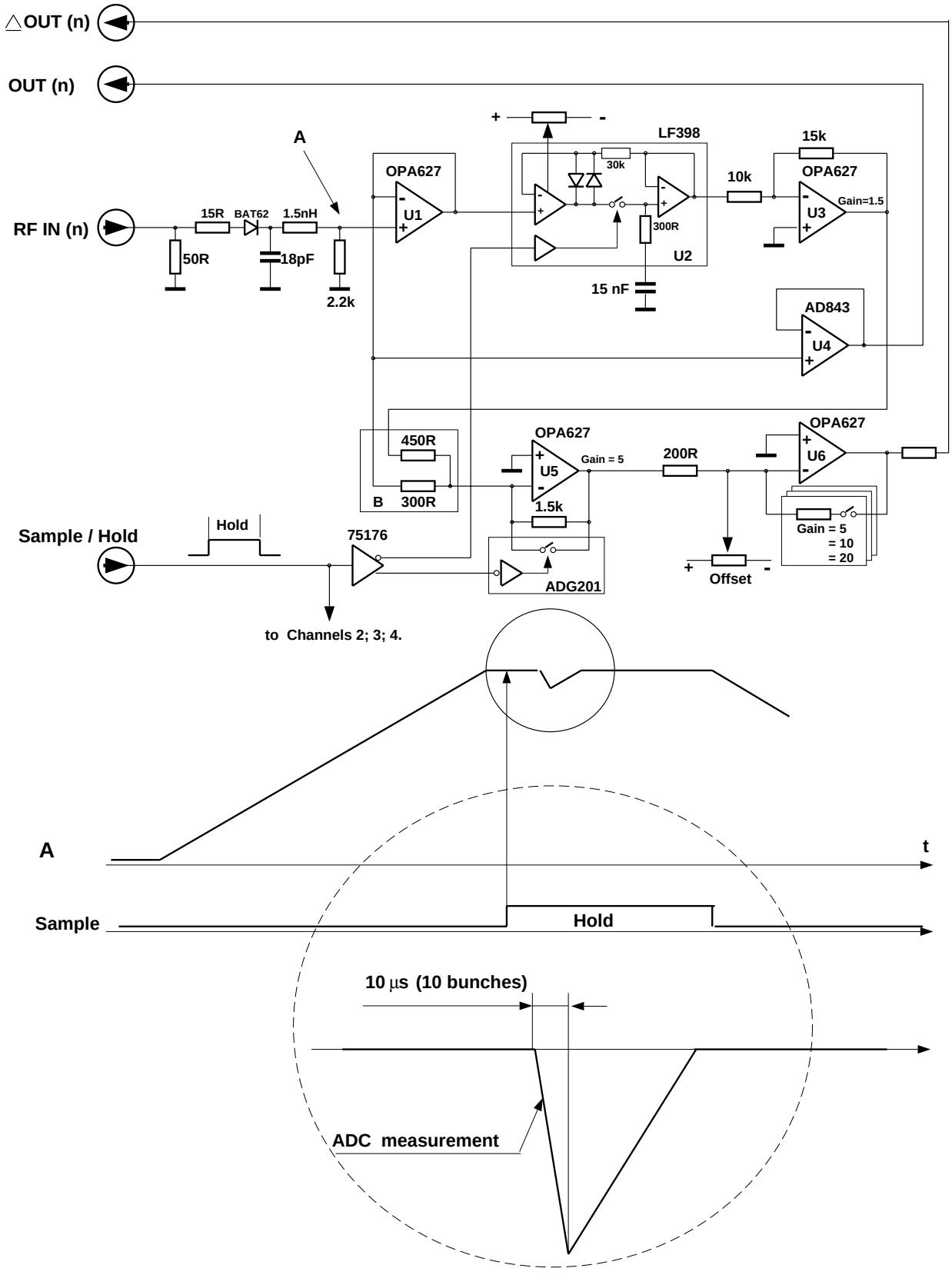


Picture 6. DSP I/O Register



- no scale
- n = 0; 1; 2; 3
- modes: - A - RF System failure
  - B - DSP failure

Picture 7. EXCEPTIONAL HANDLING with DSP I/O Register



Picture 8. Transient Detector Board (one channel)