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REAL-TIME DATA MONITORING IN THE BIG LIQUID ARGON SPECTROMETER DATA ACQUISITION SYSTEM, TAGGED NEUTRINO EXPERIMENT

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Abstract

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A procedure developed to run during inter-spill pauses in the embedded microcomputers of the Big Liquid Argon Spectrometer data acquisition system is described. It features highly integrated processes of ADC channels monitoring and unidirectional digital data path control. The aim of these operations is to ensure quality of the acquired data and to check the working parameters of the ADC cards. We give a short description of the electronic hardware structure, then outline the aim of our work and describe an algorithm of the developed programs operation.

Аннотация

Беликов С.В., Липаев В.В., Лось С.В. Оперативный контроль данных в системе сбора данных Большого жидкоаргонового спектрометра, КМН: Препринт ИФВЭ 97-34. – Протвино, 1997. – 7 с., 3 рис., 1 табл., библиогр.: 6.

Описывается процедура, выполняемая во время пауз между выводами пучка встроенными микрокомпьютерами системы сбора данных Большого жидкоаргонного спектрометра. Процедура включает связанные между собой процессы контроля состояния каналов АЦП и проверки однонаправленного цифрового канала передачи данных. Целью этих операций является обеспечение качества поступающих данных и контроль за рабочими параметрами модулей АЦП. После краткого описания электроники системы сбора данных приводится цель работы и описывается алгоритм работы созданных программ.

Introduction

BARS is a large scale liquid argon calorimeter, which is used as a target for the neutrino beam in the Tagged Neutrino experimental setup (TNE, Serpukhov) [1]. It consists of 48 ionization chambers interleaved with scintillator planes of the trigger system [2], they are housed in two cryostat vessels 4 meters in diameter and 20 meters long each. The ionization chambers are made of planes of signal strip electrodes consecutively oriented at 0° , 120° and 240° to the vertical, separated by solid ground planes. There are 48 strips (61 mm wide each) in a plane, the plane pitch is 57 mm. The detector is intended to measure released energy and its spatial distribution for the tagged neutrino interactions.

Front-end electronics [3] for 27648 signal electrodes and crates with digital read-out controllers, embedded μ-computers and other modules are located in the vicinity of the detector. Front-end modules include a full chain for ionization signal processing up to analog-to-digital conversion and are housed in 72 boxes, attached to the feedthrough flanges. There are two 6U Eurocrates with custom backplanes in each of those 72 boxes. Each crate incorporats 24 8-channel charge-to-digital conversion cards (QDC), one Selective Analog Sum card (SAS), one Calibration Distributor (CD) card and one Input-Output (I/O) card each. 24 CAMAC crates with data acquisition system (DAQ) electronics [4,5] are located in 6 racks, distributed on a path along the BARS cryostats. We use a μVAX-3300 under VMS as a central data acquisition computer.

Table 1.

Electronics type	Short description
Front-end electronics	144 crates, 3888 modules, 27648 channels; 2 μs peaking time; 11 bit, 130 μs conversion
Front-end data acquisition electronics	24 CAMAC crates, 24 μC, 240 modules; pedestal subtraction and zero-suppression; 200 μs QDC cards read-out; max. 1500 events/s or 800 events/spill
Back-end CAMAC crates	2 CAMAC crates, 27 modules

We consider a real-time test of digital electronics and technical control for the validity of the collected data being among the very important tasks for 24 Intel-8086 based μ-computers, embedded into the CAMAC crates with read-out controllers. To have reliable data from the detector with that many of electronics we should continuously check all the stages of the signal conversion along with the data collection and preprocessing.

1. BARS electronics operation

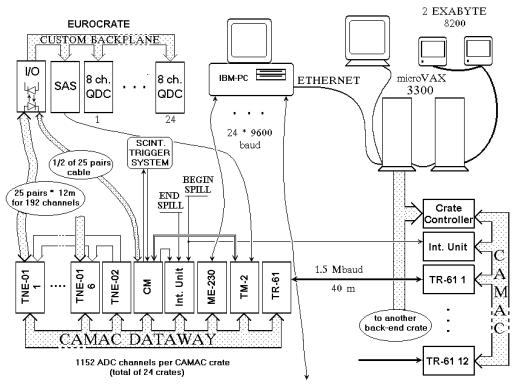

Fig. 1. BARS data acquisition system organization.

A schematic view of a CAMAC crate organization and its connections is presented in Fig. 1.

An I/O card serves as an interface between a Eurocrate and a Tagged Neutrino Experiment readout controller (TNE-01). To separate grounds of the Eurocrates with sensitive preamplifiers from the "noisy" CAMAC crates, there are opto-couplers in the I/O cards for all digital signals. The Readout Controllers located in one CAMAC crate send a common sequence of addresses to their I/O cards and receive results of the last analog-to-digit conversion from QDC card scalers. There is an arithmetic-logic block (ALB) in the TNE-01, providing pedestal subtraction and zero-suppression (if enabled). Pedestals and thresholds, individual for each channel are stored in a pedestal RAM (PRAM). The result, which exceeds the threshold, with the appended channel number is stored in an internal single-event buffer RAM (BRAM) of the TNE-01. You can see a block diagram of the readout controller in Fig. 2.

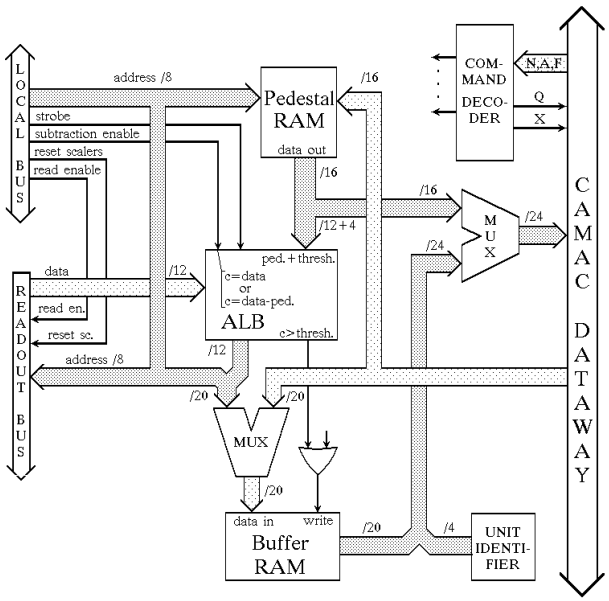

Fig. 2. Block diagram of the Readout Controller TNE-01.

There is an extra module for a group of the TNE-01 in the crate. This is a readout sequencer (TNE-02), combining common functions of the readout controllers, such as a programmable rate generator and a programmable readout channels generator. It allows for choosing readout time for one channel in a range of 500 ns - 40 μs and a range of channels you want to read from 1 to 256. A local μ-computer with a CAMAC Auxiliary Controller interface (μC ME-230) provides data accumulation and storage for the beam extraction period from 6 readout controllers housed in the crate, data control and transmission to the back-end CAMAC crates and test of the crate electronics at the inter-spill time. Communication of that local microcomputer with the host μVAX-3300 is provided by means of a pair of serial link (TR-61) modules [6]. One of them is inserted in the crate with the μ-computer and the other in one of the two crates, being under the control of the host computer. The TR-61 includes a 1Kword RAM, its content may be copied to the RAM of another TR-61 for 10 ms via a 50 ohm coaxial cable. There are two Exabyte-8200 units attached to the mVAX to store the data. For the on-line monitoring of the collected information we have an IBM-PC, connected to the host via Ethernet, it is also used to develop and load programs into the μ-computers via individual serial lines, 9600 baud.

We use a 12 bit pulse generator, driven by one of the μ-computers, to provide a relative calibration of the QDC channels and to check the signal chain continuity. Calibration signal comes to all the QDC crates of the detector, the synchro-signal is mixed with the trigger signal and is adjusted in time. There are two other signals: Begin Spill and End Spill, we use to synchronize the DAQ with the accelerator. Both of them come to Interrupt Units (IU) placed in CAMAC crates for each μ-computer and μVAX as well.

2. Electronics test

It is always important to understand, where hidden errors can happen; such things, as a μ-computer or a crate controller failure are not dangerous, as they completely stuck the system. So, while assembling the electronic hardware and during the following methodical runs, the elements of the system, where malfunctions mainly occur have been found. These are:

1. Serial Links connecting local μ-computers and the host μVAX.
2. Readout Controllers in the CAMAC crates.
3. Contacts in the cable communications between the feedthrough flanges and the QDC cards.
4. QDC cards themselves.
5. I/O cards in the Eurocrates.

Thus, almost at any stage of the datapass the data may be faked. Some origins of the errors may be easily found, as in CAMAC, where you can load predefined data and read them out, in other cases, as in QDC boxes, we have no means to do this, as the dataway is unidirectional. There is also another way to check the validity of the data, it consists in monitoring different statistical parameters, such as muon ionization peak position or relative frequency of the channel hits, etc. But it usually takes a long time to accumulate

necessary data for such analysis. So, we have tried to utilize different approaches for the on-line test programs, developed for the embedded μ-computers and the μVAX. It's worth mentioning, that all tests take place in the interspill pauses, after the data, accumulated during a beam spill have been sent to the host computer. The spill and the inter-spill duration are about 1 and 8 sec, respectively, at the IHEP 70 Gev proton synchrotron. The test volume is chosen in such a way to have a test data flux about or exceeding that of the real data.

To check a serial link-to-serial link communication we just send an extra control sum word for a 1 Kword data block. Besides, we have an extensive off-line procedure, which is used on time-to-time basis or when an error is detected. In this case the μVAX sends a data buffer or a request for a pre-defined data buffer to a μ-computer and waits for a reply. Therefore, one can determine, which of the directions of the data transmission is responsible for an error. The result of the test is controlled by the host computer.

After the data from a spill have been sent to the host μVAX, a μ-computer fulfills a series of tests, which last for several inter-spill periods. The series includes a generic test of CAMAC modules and verification of the data path integrity from the QDC registers to the Readout Controller Buffer RAM. The latter is combined with QDC channels calibration and pedestals updating.

Destinations for the generic CAMAC test are all the registers and memories in the crate, the main accent being at the Pedestal and the Buffer RAMs of the TNE readout controllers and the RAM of the serial link. We load RAMs with aperiodic data blocks, then read back and compare the memory content with the expected one to check both data bits functioning and addresses continuity.

The second part of the test includes the calibration of the BARS channels with a programmable pulse generator (PG). The μVAX sends a command to all the operating μ-computers to measure a calibration point at a certain signal amplitude with a certain statistics. On receiving this command, the μ-computer, which controls the PG, sets the amplitude and initiates as many pulses, as needed for every μ-computer to get necessary statistics. On getting the results for the current calibration point from all the μ-computers, the μVAX issues a command for processing the next point and so on, according to the list of the calibration points. While composing this list, we had several considerations in mind:

- To have all data bits combinations from each QDC channel for an explicit data path control;
- To have enough detailed information about the channel calibration curve.

Charge amplifiers, we are using, provide noise RMS deviation at the level of 11 QDC counts, so we should use not less than N=256 measurements for each point to know its position with an error within 1 count. If we choose even a quad noise RMS step for calibration (44 counts), the adjacent points still have a good overlap. It means that we expect to get each code at least once, in contrast with the six-fold RMS step, when we can expect to have missing codes. Appropriate pictures are shown in Fig. 3.

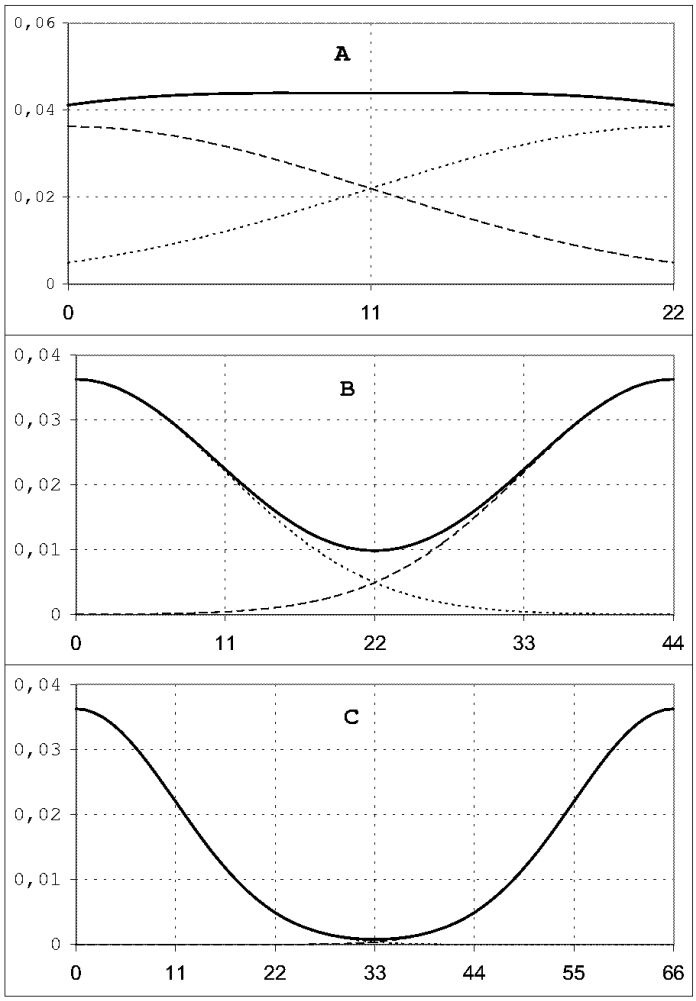

Fig. 3. Frequencies of different codes occurrence, depending on the calibration step. Calibration step to Noise RMS ratio: A: 22/11; B: 44/11; C: 66/11.

The dynamic range of our QDC converters is 2048 counts for the linear region. So, we should set not less than 46 points (2048/(11×4)) for the test purposes. When a conversion in the QDC cards has been finished, the data are fixed in the card's registers until the next conversion. We use this feature for multiple reading of the same data for the test purposes. Three different readouts permit us to control the data path and the ALB of the RC operation. We program the readout sequencer for a slow readout and store the data, then set up the fast readout and compare the results. Thereafter we load pedestals and thresholds in the PRAM, enable the pedestals subtraction and zero suppression in ALB and fulfil the third readout operation. The result is also compared with the calculated one. For the first two operations we control the order of the channel numbers (from 0 to 191) appended to the data in the readout controllers, and for the third data block we just control the monotony of the address sequence. If any discrepancy is found, a proper message is sent to the μVAX, where it is displayed and stored in an error list.

The described above procedure permits us to check:

- operation of the RAMs in the crate, where pedestals and data are stored;
- reliability of the cable connections and the presence of the amplification in the QDC-cards by analyzing the calibration curves for each channel;
- operation of every bit in the QDC-card scalers and the bus interfaces by calculating individual logical OR and AND over the data, received from each channel;
- speed at which an I/O card can reliably transfer addresses and data, this is performed by varying the fast readout speed and controlling the data correspondence to the slow readout results;
- correctness of pedestal subtraction and zero suppression in the ALB of a TNE-01.

It takes 1 to 2 inter-spill pauses to measure every calibration point and to check the calibration data. So, for the total number of 46 points it takes about 10 minutes for the full calibration and electronics test. This is also the period, when we can have the updated pedestal values for the QDC channels.

Conclusion

The developed procedure allows for a detailed control over every stage of the data transfer and preprocessing including the test of a unidirectional dataway from the front-end electronics to the CAMAC readout controllers. This is achieved by means of:

- sending predefined aperiodic data blocks;
- using certain redundancy while performing the calibration procedure;
- calculating several physical and combinatorial parameters for the acquired data.

We use this technique to reveal the malfunctions in the BARS data acquisition hardware. This permits us to have a prompt control over the operating conditions and minimizes the time we spend to find out and fix the origin of data spoiling, thus preventing the acquisition of faked information.

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